REMARKS

Claims 1-27 are pending in the application, claim 1 has been objected to for informalities, claims 1-5 and 7-15 are rejected, and claim 6 and 16-27 are withdrawn from consideration.

Claim 1 has been amended as suggested by the Examiner.

By the office action, claims 1, 8, 9, and 15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Teong (US Pat. 5,693,563) in view of Hegde et al. (US Pat. 6,136,682). The rejection is respectfully traversed.

Claim 1 recites, inter alia, An integrated circuit comprising a dielectric layer formed over a substrate, a first damascene structure in the dielectric layer, the first damascene structure comprising a bottom surface and first and second sidewalls, a first conductor located in the damascene structure, the conductor comprising a conductive material, a first liner layer lining the bottom surface and sidewalls of the first damascene structure and encapsulating the first conductor by contacting a top surface of the first conductor, the liner layer imparts a random grain orientation in the conductive material of the first conductor to improve electromigration lifetime of the first conductor, a second damascene structure in the dielectric layer, the second damascene structure comprising a bottom surface and second sidewalls and disposed above said first damascene structure, a second conductor located in the damascene structure, the conductor comprising a conductive material, a second liner layer lining the bottom surface and sidewalls of

damascene structure comprising a bottom surface and second sidewalls and disposed above said first damascene structure, a second conductor located in the damascene structure, the conductor comprising a conductive material, a second liner layer lining the bottom surface and sidewalls of the second damascene structure and encapsulating the second conductor by contacting a top surface of the second conductor, the liner layer imparts a random grain orientation in the conductive material of the second conductor to improve electromigration lifetime of the second conductor; and wherein said second liner layer is in contact with said first liner layer.

As the Examiner correctly noted, Teong does not disclose a liner layer of an amorphous character that would impart a random grain orientation to the conductive material. The Examiner has stated that it would have been obvious to one of ordinary skill in the art to use an amorphous titanium nitride layer in the invention of Teong for the disclosed intended purpose of Hegde et al. of obtaining an improved copper barrier layer. The applicant respectfully disagrees.

Hedge et al. teaches depositing a titanium nitride layer on top of a tantalum nitride layer as an excellent barrier to copper diffusion over a greater thermal range than the prior art (Col. 3, lines 10-14). In Hedge et al., it is the combination of titanium nitride on top of tantalum nitride that provides the improved barrier. Furthermore, Hedge et al. discloses that titanium nitride films are usually crystalline in nature whereby optimal copper containment is <u>not</u> obtained (Col. 1, lines 36-38). In addition, Hedge et al. discloses that titanium nitride by itself has poor adhesion to copper, and a titanium nitride barrier used in isolation comprises step coverage compared to other materials (Col. 1, lines 42-48). Therefore, Hedge et al. does not disclose the present invention

Further, one of ordinary skill in the art would not be motivated to combine Hedge with Teong because Hedge discloses that titanium nitride by itself is a poor barrier (Col. 1, lines 36-49). And, Hedge discloses using a combination of tantalum nitride and titanium nitride because a single layer is an inadequate barrier (Col. 1, lines 43-46). Therefore, Hedge teaches away from the solutions accomplished by the presently claimed invention.

Nowhere in Teong or Hedge or in the combination thereof is it disclosed or suggested to one of ordinary skill in the art to "encapsulate a conductor with a liner layer that imparts a random grain orientation in the conductive material of the conductor to improve electromigration lifetime of the conductor," or "an integrated circuit comprises a layer lining the bottom surface and sidewalls of a damascene structure and encapsulating the conductor by contacting a top surface of the conductor , and the liner layer imparts a random grain orientation in the conductive material of the conductor to improve electromigration lifetime of the conductor," as claimed in claim 1.

Thus, even if assuming, *arguendo*, that Teong can be combined with Hedge, a prima facie case of obviousness cannot be established because the combination falls short of the above claimed elements.

Claims 2-5 and 7-15 depend from claim 1. Since these dependent claims depend from independent claim 1, the dependent claims include the elements of the independent claim; Therefore, the dependent claims are allowable for the same reasons given for the independent

Claims 2-5 and 7-15 depend from claim 1. Since these dependent claims depend from independent claim 1, the dependent claims include the elements of the independent claim; Therefore, the dependent claims are allowable for the same reasons given for the independent claims.

In view of the foregoing amendment and remarks, it is respectfully submitted that all the claims now pending in the application are in condition for allowance. Early and favorable reconsideration of the case is respectfully requested.

Respectfully submitted,

By: Frank DeRosa
Reg. No. 43,584
Attorney for Applicants

F.CHAU & ASSOCIATES, LLP
1900 Hempstead Turnpike, Suite 501
East Meadow, New York 11554
Telephone: (516) 357-0091
Facsimile: (516) 357-0092

IN THE CLAIMS (Marked-up Version)

1.(Five times amended) An integrated circuit comprising:

a dielectric layer formed over a substrate;

a first damascene structure in the dielectric layer, the first damascene structure comprising a bottom surface and first and second sidewalls;

a first conductor located in the damascene structure, the conductor comprising a conductive material;

a first liner layer lining the bottom surface and sidewalls of the first damascene structure and encapsulating the first conductor by contacting a top surface of the first conductor, the liner layer imparts a random grain orientation in the conductive material of the first conductor to improve electromigration lifetime of the first conductor;

a second damascene structure in the dielectric layer, the second damascene structure comprising a bottom surface [and second] and second sidewalls and disposed above said first damascene structure;

a second conductor located in the damascene structure, the conductor comprising a conductive material;

a second liner layer lining the bottom surface and sidewalls of the second damascene structure and encapsulating the second conductor by contacting a top surface of the second conductor, the liner layer imparts a random grain orientation in the conductive material of the second conductor to improve electromigration lifetime of the second conductor; and

wherein said second liner layer is in contact with said first liner layer.